

This specification relates to 1401 systems with the latest issues of modules: the standard 1401-3 G and 1401-4 K within the 1401, and the multiplier/memory option card, 1401-13 C. The specification is liable to alteration without notice.

### Host interfaces

Specific interfaces: Data rates to/from host (kB/sec)

Apple [], //e, //e 65C02	35	Hewlett Packard 85	20
Apricot	55	IBM PC, XT, AT	142
BBC model B, B+, Master	50	RML Nimbus	62
Hewlett Packard 9816	100	DEC VAX (VMS via IEEE)	100

Generalised interfaces: RS 232 (to 19200 Baud) or IEEE 488.

### Hardware expansion

- \* Faster ADC: 130 kHz in place of standard 80 kHz maximum.
- \* Dual simultaneous sample/hold on ADC input
- \* Internal module with either 2 or 8 Mbytes of mass memory.
- \* Resistor programmable fixed input amplifiers or dynamically programmable input amplifiers and filters are available.
- \* Conversion kits are available to change hosts or to upgrade older units to the current specification.

### Analogue to digital converters (ADCs)

16 channels at 12 bit accuracy, 12 microseconds conversion. Conversion by: program, crystal clock 4 or external pulse. Options: dual sample/hold; 150 kHz ADC rate to Mass RAM.

Operating voltage range  $\pm 5$  volts. Maximum safe voltage is  $\pm 20$  volts, but no inputs should be more than 25 volts apart. The input impedance is not less than 1 M Ohm.

Standard software commands for single channel use, with 12 bit sampling, give these maximum rates. In most cases, rates can be made faster by special coding but not to more than 133 kHz except to Mass RAM, where 153 kHz is an option.

ADC data rates to ...	kHz
Memory, sole operation	83
interrupt driven	42
Mass RAM, sole operation	83
interrupt driven	47
Host, data memory *	67
fixed disc \$	67

\* 8 kHz only to the Apple \*  
\$ Measured for IBM only \$

### Digital to Analogue converters (DACs)

4 channels, 12 bit accuracy,  $\pm 5$  volts range. External brightup pulse on DAC 1 update. Double buffering available on DACs 0,1 and 2,3. Clocked conversion on DACs 1 and 3 from clocks 3 and/or 4. Output impedance less than 1 Ohm. The drive capability is 600 Ohms and the outputs are short circuit-proof. Data rates are similar to or faster than the ADC rates.

# 1401 Specification

## Five fast clocks and one calendar clock

### Clocks 0 and 1

16 bit prescaler, 16 bit counter and overflow flag for each clock.  
1 MHz internal crystal frequency source or external source (to 4MHz).  
External start, and external reading trigger on both clocks.  
Digital input change of state flag linkable to clock 0 latch.

The standard software measures event times to the nearest microsecond, at rates of up to 20 kHz on up to 8 channels. All the input times may be stored, or the data can be pre-processed to form histograms of: post stimulus response times, inter-event times, auto-correlations, or cross-correlations on one or more channels, as appropriate. The polarity of all five of the event channels can be controlled by software.

### Clock 2

3 counter/timer stages of 16 bits each plus overflow flag.  
6 different clock modes of operation includes gated operation.  
Final stage available as TTL signal.  
Linkable to digital output to allow clocked digital changes.  
1 MHz internal crystal clock or external frequency source (to 4 MHz).

One standard command offers multi-mode operation, with timing functions and a range of timed signal generation.

Another command provides precisely timed sequences of digital pulses, of microsecond accuracy and millisecond resolution, for driving external equipment, or controlling other commands within the 1401 itself!

### Clocks 3 and 4 (DAC and ADC clocks)

Each clock has two stages of 16 bits each plus overflow flag.  
Links to DAC and ADC for clocked conversion/updates.  
External trigger inputs to start the clocks.  
4 MHz internal crystal clock or external frequency source (to 4 MHz).

Signal averaging: with 12 bit data acquisition and 32 bit accumulation, up to 65,535 sweeps of over 8000 values may be summed. Using standard software, 1024 point sweeps may be captured and averaged at more than 20 times per second, or with special software, 50 times per second.

### Calendar clock

The battery-backed calendar clock can be read to the nearest second and runs for over 3 months in the absence of mains power.

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### Digital input and output

8 dedicated input lines with change of state flag and handshakes.  
8 dedicated output lines with double buffer on clock 2 facility.  
8 bidirectional lines, each user assignable to input or output.

Standard commands offer input and output of single bits, or synchronous bytes or words.

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